Conclusion

Applicants request reconsideration of the instant application in view of the foregoing remarks. Applicants submit that the pending claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

The Examiner is invited to contact the undersigned if a telephone call could help resolve any remaining issues

Respectfully submitted,

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Appendix A – Pending Claims

1. An integrated circuit device comprising:

a bond pad structure including:

a conductive pad;

a first doped region of a first conductivity type disposed in a semiconductor substrate of a second conductivity type, wherein the first doped region is underlying and surrounding the conductive pad;

a conductive region of the first conductivity type disposed in the first doped region;

a first tap region spaced apart from and surrounding a substantial portion of the first doped region, wherein the first tap region is electrically coupled to a first supply voltage;

an output driver transistor having a drain region and a source region, wherein the drain region is electrically coupled to the conductive pad; and

a second tap region surrounding the output driver transistor, wherein the second tap region is electrically and physically coupled to a second supply voltage and the source region.

2. The integrated circuit device of claim 1 wherein the first and second supply voltages are ground.

3. The integrated circuit device of claim 2 wherein the first tap region completely surrounds the first doped region.

4. The integrated circuit device of claim 1 wherein the first tap region is a

discontinuous region.

5. The integrated circuit device of claim 1 wherein a doping concentration of the first doped region is less than a doping concentration of the conductive region.

6. The integrated circuit device of claim 1 wherein the first tap region is a second doped region and the second tap region is a third doped region.

7. The integrated circuit device of claim 6 wherein the second doped region is of an opposite conductivity type than the first doped region.

8. The integrated circuit device of claim 6 wherein the third doped region is a P type doped region and the output driver transistor is an NMOS type transistor.

9. The integrated circuit device of claim 1 further including a tap region portion that is spaced apart from and surrounding the first doped region, wherein the tap region portion is decoupled from the first supply voltage to provide a predetermined resistance between the first doped region and the first supply voltage.

10. The integrated circuit device of claim 1 wherein a portion of the second tap region is integrated into the source region.

11. The integrated circuit device of claim 10 wherein the first tap region is a discontinuous region.

12. A bond pad for an integrated circuit device, the bond pad comprising:

a conductive bonding layer;

a doped region of a first conductivity type formed in a semiconductor substrate of a second conductivity type, wherein the doped region is underlying and surrounding the conductive bonding layer;

a conductive region of the first conductivity type disposed in the doped region, wherein the conductive region is underlying the conductive bonding layer and wherein the conductive region includes a surface area at least substantially equal to a surface area of the conductive bonding layer; and

a conductive tap region spaced apart from and surrounding at least a portion of the doped region, wherein a portion of the conductive tap region is electrically coupled to a supply voltage.

13. The bond pad of claim 12 wherein the supply voltage is a ground voltage and the conductive bonding layer includes a metal.

14. The bond pad of claim 12 wherein the doping concentration of the doped region is less than the doping concentration of the conductive region.

15. The bond pad of claim 12 wherein the conductive tap region is doped to be of an opposite conductivity type than the first doped region.

16. The bond pad of claim 12 further including a conductive tap region portion that is spaced apart from and surrounding the doped region, wherein the conductive tap region portion is decoupled from the supply voltage to provide a predetermined resistance between the doped region and the supply voltage.

17. The bond pad of claim 12 wherein the conductive tap region is a continuous region.

18. The bond pad of claim 17 wherein the conductive tap region completely surrounds the doped region.

19. The bond pad of claim 12 wherein the conductive tap region is a discontinuous region.

20. The bond pad of claim 19 wherein the conductive tap region substantially surrounds the doped region in a concentric-like manner.

21. The bond pad of claim 12 wherein the conductive region is polysilicon.

22. The bond pad of claim 21 wherein the conductive tap region is a doped layer positioned beneath the conductive region.

23. A transistor layout for an integrated circuit device having a bond pad, the transistor layout comprising:

a drain region having a first conductivity type doping, wherein the drain region is formed in a semiconductor substrate region having a second conductivity type doping, the drain region being electrically coupled to the bond pad;

a source region including a second conductivity type doping; and

a conductive tap region spaced proximal to and surrounding the drain region, wherein the conductive tap region is electrically coupled to a supply voltage and electrically and physically coupled to the source region, wherein a section of the conductive tap region is structurally integrated with the source region.

24. The transistor layout of claim 23 wherein the supply voltage is a ground voltage.

26. The transistor layout of claim 23 wherein the conductive tap region is spaced proximal to and completely surrounds the drain region.

27. The transistor layout of claim 23 wherein the conductive tap region is a discontinuous region.

28. The transistor layout of claim 23 further including:

a plurality of source regions, each source region of the plurality of source regions being electrically and physically coupled to the conductive tap region;

a plurality of drain regions, each drain region of the plurality of drain regions being electrically coupled to the bond pad; and

wherein the conductive tap region is spaced proximal to and surrounds at least one drain

region of the plurality of drain regions.

29. The transistor layout of claim 23 wherein the source region includes the first conductivity type doping.

30. The transistor layout of claim 23 wherein the conductive tap region is contiguous through a length of the source region.

31. The transistor layout of claim 23 further including a conductive tap region portion spaced proximal to the drain region, wherein the conductive tap region portion is electrically decoupled from the supply voltage and physically decoupled from the conductive tap region.

32. The transistor layout of claim 31 wherein the conductive tap region portion is electrically decoupled from the supply voltage and physically decoupled from the conductive tap region using a metal mask option.

33. The transistor layout of claim 23 wherein the first conductivity type doping is N type doping and the second conductivity type doping is P type doping.

34. The integrated circuit device of claim 9 wherein the tap region portion is physically separate from the first tap region.

35. The integrated circuit device of claim 16 wherein the conductive tap region portion is decoupled from the first supply voltage using a metal mask option.

36. The bond pad of claim 16 wherein the conductive tap region portion is physically separate from the conductive tap region.

37. The bond pad of claim 16 wherein the conductive tap region portion is decoupled from the supply voltage using a metal mask option.